Double-gate MOSFET based reconfigurable cells

The technology is a new style of reconfigurable cells, using the double-gate (DG) MOSFET based on independent control of gates in an asymmetric structure. A dynamic reconfigurable 4-function logic cell has been used to benchmark the architecture.

- Independent control is used to adjust the threshold voltages of all transistors so as to make them tailored to the designed logic function. The backgate uses either asymmetric oxide thickness or asymmetric workfunctions while the other cell transistors use symmetric implementation. This way a cell can either implement the logic functions $A \cdot B$ or $A + B$ or $A$ or $B$.

Advantages / Novelty

Compared to current transistor implementations, the double-gate reconfigurable cells provide one or many of the following advantages:
- reduced area
- reduced parasitic capacitance
- reduced delay through optimized routing interconnection
- reduced dynamic and static power consumption
- reconfigurable logic blocks

Current stage of development

SOI DGMOS-based reconfigurable logic cells have been designed and characterized by electrical simulation. The laboratory intends to apply the same design technique to logic cells based on silicon nanowire FETs. Besides, carbon nanotube FET based reconfigurable logic cells with 14 elementary functions have been designed. The next stage is to explore the use of graphene FETs to achieve similar functionality using a carbon-based device with a clearer integration roadmap. Eventually, a computing architecture based on clusters of matrices of logic cells has been designed as a basis for the development of a complete design platform for this novel type of architecture.

Applications

- Different transistor structures: Fin FET, Vertical DG, Planar DG, CNTFET, Si nanowire FET
- Next generation FPGA and PLD
- Reconfigurable ASIC blocks
- Standardised manufacturing process for various ASICS with end of process customization.

Intellectual property

Patent pending in PCT (FR0756487)
Priority date: July 13, 2007

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